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A Five Level Inverter Scheme using Single DC Link with Reduced Number of Floating Capacitors and Switches for Open End IM Drives

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Abstract:

This thesis presents a 5-Level inverter topology for Open-End Induction Motor drives (OEIM) by using a single DC source with solar. The open stator windings of the drive are supplied with a 3-Level Flying Capacitor inverter (FC) from one end and capacitor fed 2-Level inverter from another end. The voltage ratio of the DC link to the capacitor in 2-Level inverter is maintained at 4:1 ratio to generate five level voltage output. The capacitor in 2-Level inverter is balanced by the switching redundant vector combinations from both the inverters while the floating capacitors in the 3-Level inverter are balanced by using redundant switching states. The proposed topology gives 5-level operation with less numbers of floating capacitors and power semiconductor switches compared to other existing topologies. Also, the balancing of the capacitors is independent of load power factor and modulation index. Further, the generalization of the proposed dual inverter scheme for any n-level inverter is also included.

Index Terms—*5-Level Multilevel Inverter, Flying Capacitor (FC), Open-End Induction Motor drive (OEIM), Space Vector (SV), Pulse width Modulation (PWM).*

1. INTRODUCTION

An inverter is an electrical device that converts direct current (DC) to alternating current (AC) the converted AC can be at any required voltage and frequency with the use of appropriate transformers, switching, and control circuits. Static inverters have no moving parts and are used in a wide range of applications, from small switching power supplies in computers, to large electric utilityhigh voltage direct current applications that transport bulk power. Inverters are commonly used to supply AC power from DC sources such as solar panels or batteries. The electrical inverter is a high power electronic oscillator. It is so named because early mechanical AC to DC converters were made to work in reverse, and thus were "inverted", to convert DC to AC.

Multilevelinverters (MLI) are the most suitable alternative for high power motor drive applications. It offers several advantages over the 2-Level inverter like low voltage stress across the switches, smoother phase voltage output, lower dv/dt across the motor phase winding, ripple free shaft torque etc. Due to its attractive features, extensive research has been going on for a few decades on multilevel converters. Different multilevel topologies have been registered in literatures, among them Neutral Point Clamp (NPC) inverter, Flying Capacitor (FC) inverter and Cascaded H-bridge (CHB) are the most common. The major application field of the multilevel inverters are induction motor drives and grid tied operation.

The NPC topology requires additional numbers of clamping diodes with increase in output voltage levels. Also, it has inherent neutral point voltage balancing problem which depends on the modulation index, load current and fundamental frequency. The FC inverter requires additional numbers of floating capacitors to generate multilevel output voltage using a single DC-link. Also, special care is required to balance all these capacitors in each PWM cycle. While the CHB topology is free from the above demerits but it requires more numbers of isolated DC source which makes the total system bulky. To reduce the component count, voltage stress across the switches and switching loss in a inverter scheme, hybrid and derivative topologies have been established by combining basic MLI structures.

Apart from traditional single-fed inverters i.e. feeding drives from one side, dual-fed inverters have also been reported in literature for OEIM drives. Dual-fed inverters are more reliable compared to single-fed inverters. Under circumstances of failure of one inverter, other inverter can still be in operation with reduced number of levels. Among these, a few basic dual-fed inverters use two isolated supplies to generate multilevel output voltage, which makes the total system bulky. Dual-fed inverter schemes proposed in uses single DC source, where either inverter operates with common mode voltage being eliminated or by applying same common mode voltages from both the inverters. But these schemes reduce the number of voltage levels with a 15% reduction in output phase voltage compared to dual inverter schemes supplied from two isolated DC-link. The dual-inverter scheme proposed in uses a single DC source but obtains only a 3-Level voltage SV structure.

This paper presents a 5-level dual-fed inverter scheme for OEIM drives using a single DC source. This topology aims to eliminate the usage of bulky transformers, required for an isolated DC source in dual-inverter topologies. At the same time, it can generate fundamental phase voltage amplitude up to 0.577 times of the DC-link voltage by modulating SV based PWM technique. This topology uses a single DC source which is connected to the 3-Level inverter while the 2-Level inverter is supplied with a capacitor. All the capacitors are maintained at their nominal voltage value by selecting proper switching state for the entire modulation range. The capacitor can be charged by using phase current which eliminates the need of additional pre-charging circuit. Switching loss is also evaluated analytically and comparison with a few basic and hybrid topologies are also shown. Generalization of the proposed topology to extend up to any n-level is included. The hardware experimental results for closed loop rotor field-oriented control (FOC) and open loop V/f control during steady and transient state are included. Further the fault tolerance capability of dual inverter scheme is also

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included.

1.1. Introduction to Multilevel Inverters for IM Drives

Multilevel inverters (MLIs) have gained significant attention in the field of industrial motor drives due to their improved harmonic performance, reduced voltage stress on power devices, and enhanced efficiency. Traditional topologies such as **Diode-Clamped (Neutral Point Clamped, NPC), Flying Capacitor (FC), and Cascaded H-Bridge (CHB)** inverters have been widely used. However, these conventional designs suffer from high switch counts, complex control strategies, and capacitor voltage balancing issues.

1.2. Open-End Induction Motor (OEIM) Drives

Open-end winding induction motor (OEIM) configurations have emerged as a viable alternative for high-power industrial applications. In such systems, a dual-inverter topology is often employed, where two two-level inverters are used to synthesize higher voltage levels. This approach eliminates the need for series-connected DC-link capacitors, but it increases switch count and complexity.

1.3. Existing 5-Level Inverter Topologies

Several researchers have proposed **5-level inverter topologies** for OEIM drives, focusing on improving efficiency and reducing the number of switches and passive components. Some key approaches include:

- **Cascaded H-Bridge (CHB) Inverter:** Utilizes multiple isolated DC sources, leading to complex wiring and increased cost.
- **Diode-Clamped Inverter (NPC):** Requires additional clamping diodes, making it impractical for higher levels.
- **Flying Capacitor (FC) Inverter:** Demands multiple floating capacitors, posing voltage balancing challenges.

1.4 Recent Advances in 5-Level Inverters

Reduced Component Count Approaches: Researchers have explored methods to reduce the switch count and capacitor requirements while maintaining the output waveform quality.

Single DC-Link Topology: Some works have demonstrated the feasibility of using a single DC link instead of multiple isolated sources, simplifying the power supply system.

Hybrid Modulation Techniques: Space Vector Pulse Width Modulation (SVPWM) and modified carrier-based PWM schemes have been investigated to optimize performance.

1.5. Proposed Scheme in Comparison to Literature

The proposed **5-level inverter scheme using a single DC link with fewer floating capacitors and switches** aims to address the limitations of existing topologies by:

Minimizing the number of power switches, thereby reducing switching losses and cost.

Using a single DC link, simplifying the power circuit while maintaining performance.

Reducing the number of floating capacitors, tackling voltage balancing issues in flying capacitor inverters.

Enhancing efficiency and reliability for industrial IM drive applications.

The development of multilevel inverters with reduced component counts for open-end induction motor (OEIM) drives has been a significant area of research.

2 LITERATURESURVEY

1. In 2010 K. Sivakumar, Anandarup Das, Rijil Ramchand, Chintan Patel, and K. Gopakumar introduced a hybrid five-level inverter topology for OEIM drives. This configuration employs a two-level inverter in series with a capacitor-fed H-bridge cell on one end and a conventional two-level inverter on the other, achieving five-level output voltages with a simplified structure.
2. In 2014 Sanjiv Kumar and Pramod Agarwal proposed a nine-level inverter topology for OEIMs that reduces the number of components compared to traditional designs. The system utilizes two three-phase three-level cascade inverters to produce nine-level phase voltages. Notably, in the event of a failure in any three-level inverter, the system can bypass the faulty unit and continue operating in a three-level mode, thereby enhancing reliability.
3. 2015: S. Srinath, K. Rajambal, and M. C. Chandorkar presented a multilevel inverter system for induction motors with open-ended windings. Their approach involves feeding the motor from both ends with two-level inverters, effectively creating a five-level output. This configuration simplifies the power circuit and improves the quality of the output voltage.
4. In 2019 paper by Mriganka Ghosh Mazumdar, Apurv Kumar Yadav, K. Gopakumar, Krishnaraj R., Loganathan Umanand, and Leopoldo G. Franquelo, titled "A 5-Level Inverter Scheme Using Single DC Link With Reduced Number of Floating Capacitors and Switches for Open-End IM Drives." This work presents a 5-level inverter topology that utilizes a single DC source, supplying the open stator windings of the motor with a 3-level flying capacitor inverter on one end and a capacitor-fed 2-level inverter on the other. The voltage ratio between the DC link and the capacitor in the 2-level inverter is maintained at 4:1 to achieve the desired five-level output.
5. In 2019, another study by Rakesh R., Krishnaraj R., Apurv Kumar Yadav, K. Gopakumar, Loganathan Umanand, and Kouki Matsuse introduced "A Switched Capacitive Filter Based Harmonic Elimination Technique by Generating a 30-Sided Voltage Space Vector Structure for IM Drives." This research proposes a method to eliminate harmonics using a switched capacitive filter, generating a 30-sided voltage space vector structure suitable for induction motor drives.
6. In 2019, Mohammed Imithias, Krishnaraj R., Apurv Kumar Yadav, K. Gopakumar, Loganathan Umanand, and Carlo Cecati proposed a "Minimization of Switched Capacitor Voltage Ripple in a Multilevel Dodecagonal Voltage Space Vector Structures for Drives." This article addresses the challenge of voltage ripple in switched capacitors, presenting a strategy to minimize these ripples within multilevel dodecagonal voltage space vector structures, enhancing the performance of drive systems.These studies collectively contribute to the advancement of efficient and reliable multilevel inverter topologies for OEIM drives, focusing on reducing component counts and improving performance through innovative design and control strategies. Research on multilevel inverters for open-end induction motor (OEIM) drives has led to various innovative topologies aimed at

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reducing component counts and enhancing performance. Here are some notable contributions:

7. 2019: Rakesh R., Krishnaraj R., Apurv Kumar Yadav, K. Gopakumar, Loganathan Umanand, and Kouki Matsuse introduced a harmonic elimination technique for induction motor drives. Their method employs a switched capacitive filter to generate a 30-sided voltage space vector structure, effectively reducing harmonic distortion.

8. 2019: Mohammed Imithias, Krishnaraj R., Apurv Kumar Yadav, K. Gopakumar, Loganathan Umanand, and Carlo Cecati addressed the issue of voltage ripple in switched capacitors within multilevel dodecagonal voltage space vector structures. They proposed a strategy to minimize these ripples, thereby enhancing the performance and reliability of drive systems.

9. In 2020 K. Sivakumar, Anandarup Das, Rijil Ramchand, Chintan Patel, and K. Gopakumar presented a fault-tolerant five-level inverter topology for OEIM drives using a single DC link. The design features a primary inverter (a two-level inverter cascaded with a capacitor-fed H-bridge) on one end and a secondary capacitor-fed two-level inverter on the other, ensuring continued operation despite component failures.

10. In 2022 Suganya and Ravichandran S. developed a multilevel inverter topology for induction motor drives capable of continuous operation at lower power levels. Their design increases voltage and power by adding levels in a symmetrical circuit and employs Sinusoidal PWM to reduce harmonics, thereby improving overall system performance.

3. PROPOSEDMETHODOLOGY

PROPOSED INVERTER TOPOLOGY

The proposed 5-Level inverter scheme having minimum components count is shown in Fig. 4.1 along with OEIM drive. The drive is powered by a 3-Level FC inverter from one end as primary inverter and a 2-Level inverter from another end as secondary inverter. In this scheme the primary inverter is fed with a DC source of voltage rating Vdc and the secondary inverter is fed with a floating capacitor whose voltage is maintained at Vdc/4. The floating capacitors in the primary inverter are maintained at a voltage of Vdc/2. The pole voltages of primary inverter (VAO, VBO, VCO) can take values of 0, Vdc/2, Vdc. The secondary inverter pole voltages (VA0O0 , VB0O0 , VC0O0) can take values 0 or Vdc/4. The phase voltage across the induction machine winding is governed by the equation

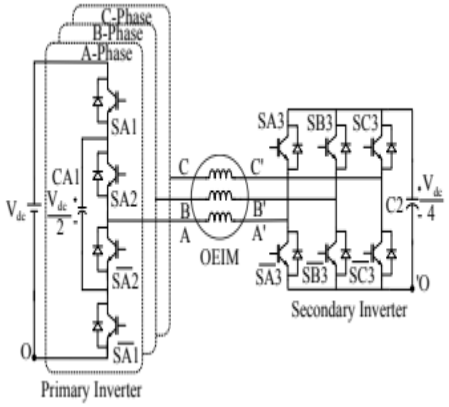

Fig. 3.1. Power circuit diagram of the proposed 5-Level inverter scheme

$$V_{AA'} = V_{AO} - V_{A'O'} + V_{OO'} \quad (1)$$
$$V_{BB'} = V_{BO} - V_{B'O'} + V_{OO'} \quad (2)$$
$$V_{CC'} = V_{CO} - V_{C'O'} + V_{OO'} \quad (3)$$

In the above equations VOO0 is the common mode voltage. As the point O and O' are isolated from each other, there is no path for common mode current to flow . The voltage stress across each switch in the primary inverter during off state is Vdc/2 and that of the secondary inverter is Vdc/4. In Fig. 1 Sxn and Sxn are the complimentary pair of switches, where 'x' is A, B orCand'n'is1,2or3.

3.2 PRINCIPLE OF OPERATION

In the proposed inverter scheme, the output of the primary inverter will generate a 3-Level SV structure of radius Vdc and secondary inverter will generate a 2-Level SV structure of radius Vdc/4 as shown in Fig. 3.2. The output voltage of the primary inverter in SV domain is given by

$$\vec{V_1} = V_{AO} + V_{BO}\angle 120^\circ + V_{CO}\angle 240^\circ \quad (4)$$

Whereas for secondary inverter defined as

$$\vec{V_2} = V_{A'O'}\angle 180^\circ + V_{B'O'}\angle 300^\circ + V_{C'O'}\angle 60^\circ \quad (5)$$

he 5-Level SV structure is generated by superimposing the 2- Level SV structure with the 3-Level SV structure. The effective voltage across motor phase −→V winding is given by −→V1+ −→V2 i.e.

Fig. 3.2(c) shows that the construction of 5-Level SV structure

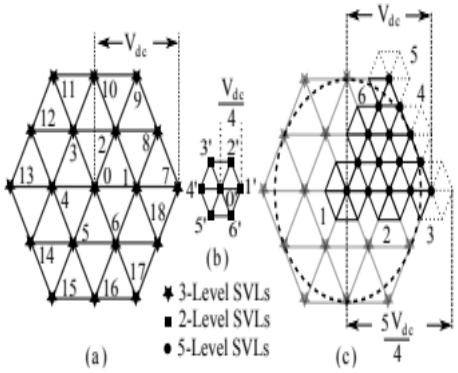

Fig.3.2. Generation of 5-Level SV structure: (a) 3-Level SV structure, (b) 2-Level SV structure,(c) 5-level SV structure.

by superimposing 2-Level SVs of radius Vdc/4 over the 3-Level SV structure of radius Vdc for 60◦ of the hexagon. Here we can not generate reference vector beyond the circle i.e.magnitude of the reference can have a maximum value 0.866Vdc beyond which the secondary capacitor voltage cannot be balanced. The reason is discussed in Section B

Total 103 unique vector combinations are possible from secondary and primary side for generating total 61 space vector locations (SVLs) in 5-Level SV structure. Fig. 3.3 and Table 3.I shows in detail the formation of 5-Level SVs by the combinations of primary and secondary SVs for 60◦ region of the 5-Level SV structure. Fig. 3.3 shows that the SVLs marked with dot have two possible combinations, while SVLs marked with

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star have only one possible combination (where zero vector applied from secondary inverter side).

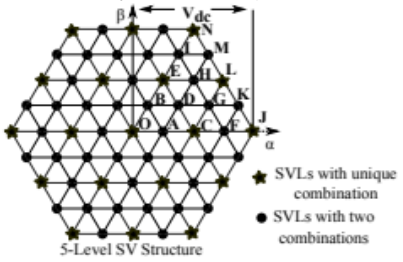

Fig. 3.3. Combinations of SV from primary and secondary inverter for generation each SVL in 5-Level SV structure.

3.3 Capacitor Voltage Balancing

To generate reference voltage, vector nearest possible SVs from 5-level SV structure have to switch. Now for each selected SV from 5-Level SV structure, there are two possible combinations (except star marked points Fig. 3.3) of SV from primary and secondary side. In order to balance all the capacitor voltages, proper vector combination have to select from primary and secondary side inverter corresponding to each selected SV from 5-Level structure. Hence, to generate switched average reference voltage vector, considering the current direction in three-phases and the secondary inverter capacitor voltage, first secondary SV will be chosen and then corresponding primary SV will be selected. Current through capacitor (C2) in secondary inverter is governed by equation

$$I_{C2} = I_a * f(SA3) + I_b * f(SB3) + I_c * f(SC3) \qquad (7)$$

Where f(SA3), f(SB3), f(SC3) are the switching function for the secondary inverter switches SA3, SB3, SC3 and can take values f(Sx3) = 1 when switch Sx3 is on and f(Sx3) = 0 when switch Sx3 is off and 'x' is A, B or C.

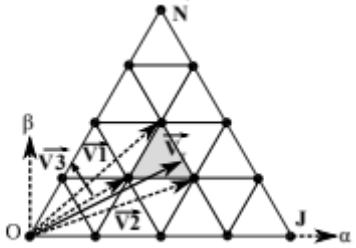

Fig. 3.4. Generation of reference voltage vector by equivalent 5-Level SV of the dual inverter system.

It can be seen from Fig. 4.4 that to generate the reference vector −→Vr, nearest SVs −→V 1, −→V 2 and −→V 3 have to switch from equivalent 5-level SV structure.Now, available SV combinations from primary and secondary inverter for composing equivalent 5-Level SV −→V 1 are (a) −→02 from primary side and −−→0'4' from secondary side (Fig. 5(a)) or (b) −→08 from primary side and −−→0'1' from secondary side (Fig. 5(b)) and corresponding switching state in the secondary inverter for SV −−→0'1' and −−→0'4' are shown in Fig. 6. Likewise, 5-Level space vector −→V 2 and −→V 3 can also be composed two possible ways by applying proper SV combination from primary and secondary inverter side.

3

TABLE 3.I
Generation of 5-level svs by combination of primary and secondary inverter svs

Combined 5-Level SV	SV from Primary Inverter	SV from Secondary Inverter
OA	01	0'1'
	0	0'4'
OB	02	0'2'
	0	0'5'
OC	01	0'
OD	01	0'6'
	02	0'3'
OE	02	0'
OF	01	0'4'
	07	0'1'
OG	01	0'5'
	08	0'2'
OH	02	0'4'
	08	0'1'
OI	09	0'2'
	02	0'5'
OJ	07	0'
OK	08	0'3'
	07	0'6'
OL	08	0'
OM	08	0'6'
	09	0'3'
ON	09	0'

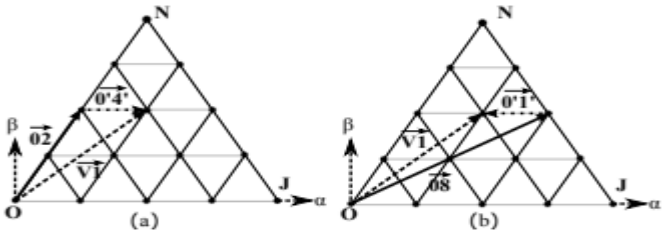

Fig. 3.5. Synthesization of 5-Level SV −→V 1 by primary and secondary SV as (−→02 + −−→0'4') or as (−→08 + −−→0'1').

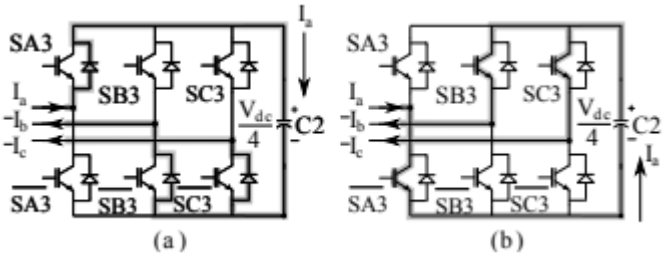

Fig.3.6. Secondary floating capacitor (a) charging for switching of SV −−→0'1', (b) discharging for switching of SV −−→0'4'.

Let assume any arbitrary current direction in three phases like, Ia is positive and Ib, Ic are negative and also consider secondary capacitor voltage is below the nominal value. For the above condition, during the instant when SV −→V 1 need to switch for generating −→Vr, vector −−→0'1' from secondary side should be switched to charge the capacitor (Refer to equation (7)) and corresponding primary vector −→08 will be switched. Similarly, with the above mentioned current direction, if the

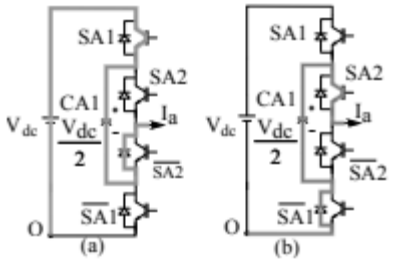

Fig. 3.7. Switching state for pole voltage VAO = Vdc/2, Primary inverter floating capacitor (a) charging, (b) discharging with the positive phase current Ia.

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secondary capacitor voltage is above the nominal value, then vector −−→0'4' will be switched from secondary side to discharge the secondary capacitor along with vector −→02 from primary side. For the considered current direction, the secondary capacitor is charging with phase current Ia when secondary vector −−→0'1' is switched Fig. 4.6(a) and the secondary capacitor is discharging by phase current Ia with the switching of vector −−→0'4' Fig. 4. 6(b). In 5-Level SV structure (Fig. 3.3) only one SV combination is available for SVLs marked in star but at those locations zero vector are switched from secondary inverter. Hence, the secondary side capacitor will be unaffected. So, it is possible to balance the secondary capacitor in every SVLs in 5-level SV structure by proposed switching strategy. f magnitude of the reference voltage vector goes beyond the dotted circle (Fig. 3.2) then we can not charge back the secondary floating capacitor as there is only one vector combination available from primary and secondary inverter. At those points active SV will be applied from secondary inverter with the corresponding SV from Primary inverter and hence secondary capacitor will be discharged and due to lack in charging states (i.e. vector redundancies) we can not charge it back. So, linear operation zone of the inverter scheme is limited up to the dotted circle as shown in Fig. 2. Primary side floating capacitors will be affected only when pole voltage Vdc/2 is applied from the primary inverter. Considering positive direction of current (Fig.3.7), the floating capacitor can be either charged by applying switching redundancy (Vdc-Vdc/2) or discharged by applying (0+Vdc/2) while generating a pole voltage of Vdc/2. This capacitor current can be written as

$$I_{Cx1} = f(Sx1) * I_x - f(Sx2) * I_x \qquad (8)$$

Where f(Sx1) and f(Sx2) are the switching functions for the primary inverter switches Sx1 and Sx2 and 'x' is A, B or C and Ix is the phase current.

Modulation Technique

The proposed inverter scheme uses Level-Shifted Carrier based PWM (LSC-PWM) for modulating its switches. In this case four level shifted carrier signal are used to compare with the modulating signal. Here modulating signal (Vr) is scaled between 0 to 4 as

$$V_{ref} = 2 + (V_r * 2)/V_{dc} \qquad (9)$$

then it is compared with the carrier signals. However, reference signal is decomposed to integer and fractional part as

$$V_{ref} = V_{int} + V_{frac} \qquad (10)$$

Vint is the nearest integer less than or equal to Vref and it can take values of 0, 1, 2, 3 and Vf rac lies in the interval [0,1) (Fig. 4.8(a)). This Vint and Vf rac information from all the three phases gives a particular SV from equivalent 5- Level SV structure and the time duration for which that SV will be switched. Now, depending upon the current direction and secondary capacitor voltage, the 5-Level space vector will be synthesized by 2-Level and 3-Level SV generated by secondary and primary inverter respectively.

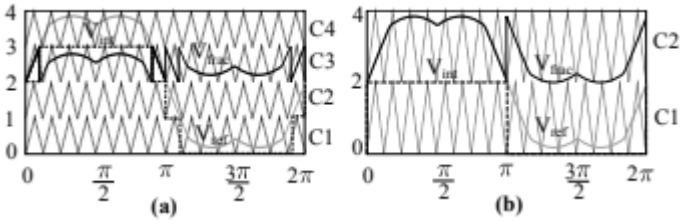

Fig. 3.8. Modulation technique: (a) during normal operation, Vref reference signal,C1-C4 are the four carriers, Vint integer component and Vfrac fractional component of reference voltage.(b) during fault condition, Vref reference phase voltage,C1 and C2 are the two carriers, Vint integer component and Vfrac fractional component of reference voltage

3.4 Inverter Operation

During Fault In the proposed inverter scheme, the OEIM drive is fed by two inverters namely primary inverter and secondary inverter (Fig. 3.1) . Primary inverter is supplied from a DC source and it supplies the required active power for the drive operation. The secondary inverter is capacitor fed inverter which is used to generate more of number of voltage levels. In case of power switch failure in secondary inverter, the drive can still be in operation with secondary inverter bypassed (zero vector will be applied from the secondary inverter). As the DC source is connected with the primary inverter, the drive can be operated at full modulation index and rated power during the fault condition. The switch in secondary inverter can be faulted with either being short circuited or open circuited. As there are 6 switches in secondary inverter, a total of 2 6 conditions are possible for fault. These possibilities can be broadly classified into four categories (a) Single switch short circuit (S.C.) fault, (b) Single switch open circuit (O.C.) fault, (C) Phase leg short circuit fault, (d) Phase leg open circuit fault. The proposed drive scheme can still be in operation in all the above mentioned fault cases except during phase leg O.C. fault because during this fault the secondary inverter cannot be bypassed. During the fault condition, the LSC-PWM method will be changed from 5-Level to 3-Level scheme (4.8(b)) with only two level shifted carrier. Switching pulses are provided only for primary inverter while in secondary inverter, either all the top switches or all the bottom switches are turned on. During the fault, the primary inverter (3-Level FC) applies three pole voltage (VAO) levels of 0, Vdc/2 and Vdc from the phase terminals. Hence the proposed scheme is more reliable compared to traditional single-fed inverter schemes.

3.5 SWITCHING LOSS CALCULATION AND COMPARISON WITH OTHER TOPOLOGIES

The switching loss for the proposed converter is calculated for different frequencies of operation for a three phase 15kW, 415V, 50Hz OEIM drive. This loss is comprised of the primary and secondary inverter switching loss during turning on and off the power IGBT device. For loss calculation the DC bus voltage is taken as 560V corresponding to phase voltage rms value 240V and peak phase current is taken as 20A. Switching loss is calculated for SKM100GB12T4 IGBTs and anti-parallel diodes at the time of their switching and averaged over the fundamental period. This loss can be calculated by following equation

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$$P = (\sum_{N} E_{test} * (I/I_{test})^{(K_i)} * (V/V_{test})^{(K_v)} * \alpha_T) * f_{freq} \quad (11)$$

Where N is the number of switching instant in one fundamental period, ff req is the fundamental frequency, V is the voltage stress across the device during off condition and I is the current through the switch. Etest, Itest, Vtest are the values taken from data sheet and Ki , Kv and αT are the constants given in data sheet. Switches of the primary inverter are switching

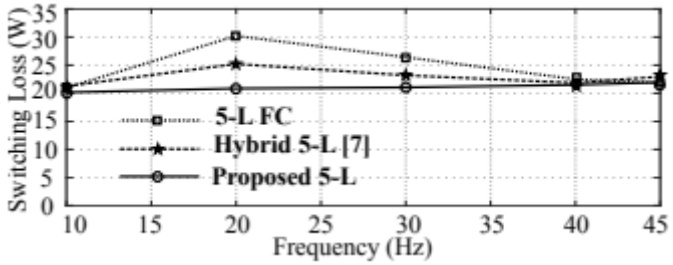

Fig. 3.9. Switching loss comparison of the proposed topology with FC and Hybrid topology .

Almost half that of switches of the secondary inverter. Hence switching loss is largely reduced due to lower switching frequency in primary inverter switches which blocks Vdc/2 than the switches in secondary inverter which blocks Vdc/4. Also switching loss comparison at different frequencies of operation is done analytically with other 5-Level topologies like 5-level FC and hybrid 5-level topology and is shown in Fig.3. 9. During switching loss comparison in all the cases switching frequencies are chosen such that the capacitor voltage peak peak ripple remains within 5% of their nominal value with the above mentioned load condition Conventional 5-Level NPC and FC inverter requires extra clamping diodes and floating capacitors respectively for their implementation. Also conventional NPC suffers from neutral point unbalancing problem at higher modulation indices. While a CHB inverter requires less amount of components but it requires additional number of isolated DC sources. This topology requires total 18 switches among them 12 switches have voltage blocking capability of Vdc/2 and rest 6 switches of Vdc/4. Capacitors of primary inverter have voltage rating of Vdc/2 whereas secondary side capacitor holds only Vdc/4. Also, all the capacitors are balanced in each PWM cycle irrespective of modulation index and load power factor. The detail comparison in terms of isolated DC source usage, component and switch counts among a few inverter topologies with the proposed topology is shown in Table 3.2.

3.6 GENERALIZATION OF THE PROPOSED INVERTER SCHEME

The proposed dual inverter scheme can be extended to any number of levels by modifying primary inverter and maintaining secondary 2-Level inverter capacitor voltage accordingly.The proposed dual inverter scheme can be generalized for a n-Level inverter where primary inverter will give (n2) pole voltage levels and the secondary 2-Level inverter capacitor voltage should be maintained at Vdc/(2 ∗ (n − 3)) (Fig. 3.10) where Vdc is the DC-link voltage. The primary inverter capacitors can be balanced by switching redundancies where as secondary inverter floating capacitor can be balanced by SV redundancies. With increase in phase voltage level the nominal value of the secondary capacitor voltage will reduce that reduces switching loss in the secondary 2-Level inverter. For an instance, to construct a 7-Level dual inverter, primary

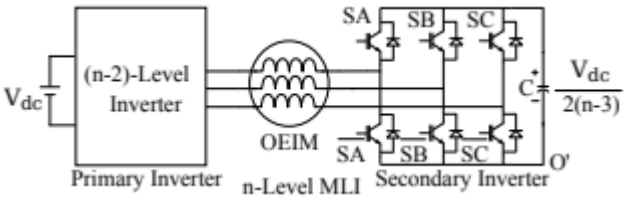

Fig. 3.10. Generalization of the proposed dual inverter scheme

inverter should be a 5-Level inverter fed with DC-link voltage Vdc and the nominal voltage of the secondary 2-Level inverter capacitor will be Vdc/8.

4 CONCLUSION

This project proposes a 5-Level inverter scheme with reduced components count for OEIM drive . The proposed scheme requires only one DC source of voltage Vdc and three capacitor of voltages Vdc/2 for primary FC inverter and only one floating capacitor of voltage Vdc/4 for secondary 2-Level inverter. All the floating capacitor voltages are balanced in each PWM cycle irrespective of load power factor and modulation index. This feature enables to use low value of capacitors in medium to high power drives applications. The capacitors can be charged by the phase current during starting hence no capacitor recharging circuit is required. Also, single DC source enables back to back power flow. The low voltage switches in secondary inverter are switching more times compared to high voltage switches in primary inverter in each fundamental cycle which reduces switching loss of the overall system. Switching loss for this topology is also compared with some of the existing topologies. Usage of single DC source and low valued capacitors makes it compact and light weight. Further during fault condition the converter can be operated as a three level inverter up to full modulation index. Generalization of the proposed topology is also included, which can be applied to extend the proposed dual inverter scheme to any n-Level inverter. Above mentioned features makes the proposed system more reliable and suitable for application in electric vehicle, industrial motor drives etc.

FUTURE SCOPE:

In further, we proposed new technique i.e, fuzzy logic controller for reduction of the harmonics under distortions voltages. The actual grid code requirements for the grid connection of distributed generation systems, mainly voltage levels with long durations and Harmonics situations at switches

REFERENCES

[1] Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, “Recent advances and industrial applications of multilevel converters,” IEEE Transactions on Industrial Electronics, vol. 57, DOI 10.1109/TIE.2010.2049719, no. 8, pp. 2553–2580, Aug. 2010.

[2] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped pwm inverter," IEEE Transactions on Industry Applications, vol. IA-17, DOI 10.1109/TIA.1981.4503992, no. 5, pp. 518–523, Sep. 1981.

[3] S. Ogasawara and H. Akagi, "Analysis of variation of neutral point potential in neutral-point-clamped voltage source pwm inverters," in Conference Record of the 1993 IEEE Industry Applications Conference Twenty-Eighth IAS Annual Meeting, DOI 10.1109/IAS.1993.299015, pp. 965–970 vol.2, Oct. 1993.

[4] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," IEEE Transactions on Industrial Electronics, vol. 57, DOI 10.1109/TIE.2009.2032430, no. 7, pp. 2219– 2230, Jul. 2010.

[5] S.-G. Lee, D.-W. Kang, Y.-H. Lee, and D.-S. Hyun, "The carrier-based pwm method for voltage balance of flying capacitor multilevel inverter," in 2001 IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230), vol. 1, DOI 10.1109/PESC.2001.954006, pp. 126–131 vol. 1, Jun. 2001.

[6] R. Teodorescu, F. Blaabjerg, J. K. Pedersen, E. Cengelci, and P. N. Enjeti, "Multilevel inverter by cascading industrial vsi," IEEE Transactions on Industrial Electronics, vol. 49, DOI 10.1109/TIE.2002.801069, no. 4, pp. 832–838, Aug. 2002.

[7] P. Roshankumar, P. P. Rajeevan, K. Mathew, K. Gopakumar, J. I. Leon, and L. G. Franquelo, "A five-level inverter topology with single-dc supply by cascading a flying capacitor inverter and an h-bridge," IEEE Transactions on Power Electronics, vol. 27, DOI 10.1109/TPEL.2012.2185714, no. 8, pp. 3505–3512, Aug. 2012.

[8] N. D. Dao and D. Lee, "Operation and control scheme of a five-level hybrid inverter for medium-voltage motor drives," IEEE Transactions on Power Electronics, vol. 33, DOI 10.1109/TPEL.2018.2811182, no. 12, pp. 10 178–10 187, Dec. 2018.

[9] H. Wang, L. Kou, Y. Liu, and P. C. Sen, "A seven-switch fivelevel active-neutral-point-clamped converter and its optimal modulation strategy," IEEE Transactions on Power Electronics, vol. 32, DOI 10.1109/TPEL.2016.2614265, no. 7, pp. 5146–5161, Jul. 2017.

[10] P. P. Rajeevan and K. Gopakumar, "A hybrid five-level inverter with common-mode voltage elimination having single voltage source for im drive applications," IEEE Transactions on Industry Applications, vol. 48, DOI 10.1109/TIA.2012.2226197, no. 6, pp. 2037–2047, Nov. 2012.

[11] A. Edpuganti and A. K. Rathore, "New optimal pulsewidth modulation for single dc-link dual-inverter fed open-end stator winding induction motor drive," IEEE Transactions on Power Electronics, vol. 30, DOI 10.1109/TPEL.2014.2353415, no. 8, pp. 4386–4393, Aug. 2015.

[12] V. F. Pires, D. Foito, and J. F. Silva, "Fault-tolerant multilevel topology based on three-phase h-bridge inverters for open-end winding induction motor drives," IEEE Transactions on Energy Conversion, vol. 32, DOI 10.1109/TEC.2017.2693563, no. 3, pp. 895–902, Sep. 2017.